U.S. PATENT APPLICATION

FOR

FRONT SIDE SEAL TO PREVENT GERMANIUM OUTGASSING

Inventors: Eric N. Paton
Haihong Wang
Qi Xiang

FRONT SIDE SEAL TO PREVENT GERMANIUM OUTGASSING

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

[0001] The present application is a continuation-in-part application of U.S. Application Serial No. ____________, filed on _________ by Ngo et al., entitled "Shallow Trench Isolation For Strained Silicon Process" (Attorney Docket No. 39153/639/HO963) and assigned to the Assignee of the present application.

FIELD OF THE INVENTION

[0002] The present invention relates generally to integrated circuit (IC) fabrication. More particularly, the present invention relates to a design for and a method of reducing contamination during IC fabrication on substrates and layers containing germanium.

BACKGROUND OF THE INVENTION

[0003] Strained silicon (SMOS) processes are utilized to increase transistor (MOSFET) performance by increasing the carrier mobility of silicon, thereby reducing resistance and power consumption and increasing drive current, frequency response and operating speed. Strained silicon is typically formed by growing a layer of silicon on a silicon germanium substrate or layer. Germanium can also be implanted, deposited, or otherwise provided to silicon layers to change the lattice structure of the silicon and increase carrier mobility.

[0004] The silicon germanium lattice associated with the germanium substrate is generally more widely spaced than a pure silicon lattice, with spacing becoming wider with a higher percentage of germanium. Because the silicon lattice aligns with the larger silicon

germanium lattice, a tensile strain is created in the silicon layer. The silicon atoms are essentially pulled apart from one another. Relaxed silicon has a conductive band that contains six equal valance bands. The application of tensile strength to the silicon causes four of the valance bands to increase in energy and two of the valance bands to decrease in energy. As a result of quantum effects, electrons effectively weigh 30 percent less when passing through the lower energy bands. Thus, lower energy bands offer less resistance to electron flow.

[0005] In addition, electrons meet with less vibrational energy from the nucleus of the silicon atom, which causes them to scatter at a rate of 500 to 1,000 times less than in relaxed silicon. As a result, carrier mobility is dramatically increased in strained silicon compared to relaxes silicon, providing an increase in mobility of 80 percent or more for electrons and 20 percent or more for holes. The increase in mobility has been found to persist for current fields up to 1.5 megavolt/centimeter. These factors are believed to enable device speed increase of 35 percent without further reduction of device size, or a 25 percent reduction in power consumption without reduction in performance.

[0006] The use of germanium in SMOS processes can cause germanium contamination problems for IC structures, layers, and equipment. In one example, germanium outgassing or outdiffusion can contaminate various components associated with the fabrication equipment and integrated circuit structures associating with the processed wafer. Further, germanium outgassing can negatively impact the formation of thin films. In addition, germanium outdiffusion can cause germanium accumulation or "pile-up" at the interface of the liner, thereby causing reliability issues for the STI structure. In another example, germanium resputtering can cause contamination. Germanium

resputtering can occur when the IC substrate is subjected to implants, cleaning and doping steps. For example, providing dopants for the source and drain regions can cause germanium resputtering.

[0007] Thus, there is a need for an SMOS process which reduces germanium contamination. Further, there is a need for a process of forming source and drain regions that does not promote germanium contamination. Further still, there is a need for an SMOS process which reduces germanium resputtering. Yet further, there is a need for a process and structure that reduces germanium outgassing. Even further, there is a need for a method of siliciding and a transistor architecture which avoids germanium resputtering.

SUMMARY OF THE INVENTION

[0008] An exemplary embodiment relates to a method of manufacturing an integrated circuit. The integrated circuit includes a gate structure above a substrate that includes germanium. The method includes forming a first layer above the gate structure and above the substrate, forming a second layer above the first layer, and doping source and drain regions through the first layer and the second layer. Germanium back sputtering is reduced by the method.

[0009] Yet another exemplary embodiment relates to a method of forming source and drain regions in a strained semiconductor layer. The method includes providing a first layer comprising at least one of silicon nitride and silicon dioxide above the strained semiconductor layer, providing a second layer above the first layer, and implanting non-neutral dopants into the strained semiconductor layer. The second layer contains nitrogen, titanium, tantalum or carbon. The method also includes annealing the strained semiconductor layer.

[0010] Still another exemplary embodiment relates to a method of fabricating a transistor in a germanium containing layer. The method includes providing a gate structure above the germanium containing layer, providing a first layer of insulative material in a low temperature process above the germanium containing layer, doping to form source and drain regions, and annealing to activate dopants in the source and drain regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements; and

[0012] FIGURE 1 is a flow diagram showing a fabrication process for a germanium-containing IC substrate in accordance with an exemplary embodiment;

[0013] FIGURE 2 is a cross-sectional view schematic drawing of a portion of the IC substrate used in the process illustrated in FIGURE 1, the IC substrate including a lithographic feature above a gate stack above a strained silicon layer above a silicon germanium substrate;

[0014] FIGURE 3 is a cross-sectional view of the portion illustrated in FIGURE 2, showing a gate structure formation step;

[0015] FIGURE 4 is a cross-sectional view of the portion illustrated in FIGURE 3, showing a coating removal step;

[0016] FIGURE 5 is a cross-sectional view of the portion illustrated in FIGURE 4, showing a buffer layer deposition step;

[0017] FIGURE 6 is a cross-sectional view of the portion illustrated in FIGURE 5, showing a sealing layer deposition step; and

[0018] FIGURE 7 is a cross-sectional view of the portion illustrated in FIGURE 6, showing a doping step.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] FIGURES 1 through 7 illustrate a method of manufacturing an integrated circuit (IC) in accordance with an exemplary embodiment. The method and IC structure illustrated in FIGURES 1 through 7 reduces the germanium contamination during various fabrication processes, including doping. The process includes at least one sealing layer that reduces germanium outdiffusion and back sputtering and can be used as a part of any process that seeks to avoid germanium contamination. Advantageously, the process reduces germanium contamination of fabrication equipment and IC structures associated with silicon germanium substrates and strained silicon or semiconductor layers.

[0020] Referring to FIGURES 2 through 7, a cross-sectional view of a portion 12 of an integrated circuit (IC) is illustrated. Portion 12 (FIGURE 2) is subjected to process 100 (FIGURE 1) to form an IC. The IC can include a transistor with a gate structure and a source and drain region as explained below. Germanium contamination can be reduced through an advantageous process and transistor architecture. The architecture uses at least one sealing layer to prevent germanium from adversely affecting the formation of IC devices.

[0021] In FIGURE 2, portion 12 includes a strained silicon layer 16 provided over a semiconductor substrate 14 or a germanium containing layer or substrate. Substrate 14 can be provided above a substrate 13.

[0022] Substrate 13 is optional and portion 12 can be provided with substrate 14 as the bottom-most layer. Substrate 13 can

be the same material or a different material than substrate 14. In one embodiment, substrate 13 is a semiconductor substrate such as a silicon substrate upon which silicon germanium substrate 14 has been grown. In another embodiment, substrates 13 and 14 are not included and the substrate is comprised of layer 16. In such an embodiment, layer 16 can be a silicon germanium substrate or a strained silicon substrate.

[0023] Portion 12 can be any type of semiconductor device, or portion thereof, made from any of the various semiconductor processes such as a complementary metal oxide semiconductor (CMOS) process, a bipolar process, or another semiconductor process. Portion 12 may be an entire IC or a portion of an IC including a multitude of electronic component portions.

[0024] Substrate 14 is preferably silicon germanium or another semiconductor material including germanium, and can be doped with P-type dopants or N-type dopants. Substrate 14 can be an epitaxial layer provided on a semiconductor or an insulative base, such as substrate 13. Furthermore, substrate 14 is preferably a composition of silicon germanium ($Si_{1-x}Ge_x$, where X is approximately 0.2 and is more generally in the range of 0.1-0.4). Substrate 14 can be grown or deposited.

[0025] In one embodiment, substrate 14 is grown above substrate 13 by chemical vapor deposition (CVD) using disilane (Si_2H_6) and germane (GeH_4) as source gases with a substrate temperature of approximately 650°C, a disilane partial pressure of approximately 30 mPa and a germane partial pressure of approximately 60 mPa. Growth of silicon germanium material may be initiated using these ratios, or, alternatively, the partial pressure of germanium may be gradually increased beginning from a lower pressure or zero pressure to form a

gradient composition. Alternatively, a silicon layer can be doped by ion implantation with germanium, or other processes can be utilized to form substrate 14. Preferably, substrate 14 is grown by epitaxy to a thickness of less than approximately 5000 Å (and preferably between approximately 1500 Å and 4000 Å).

[0026] A strained silicon layer 16 is formed above substrate 14 by an epitaxial process. Preferably, layer 16 is grown by CVD at a temperature of 600-800°C. Layer 16 can be a pure silicon layer and may have a thickness of between approximately 50 and 150 Å.

[0027] The substrate for portion 12 can be a semiconductor substrate such as silicon, gallium arsenide, germanium, or another substrate material. The substrate can include one or more layers of material and/or features such as lines, interconnects, vias, doped portions, etc., and can further include devices such as transistors, microactuators, microsensors, capacitors, resistors, diodes, etc. The substrate can be an entire IC wafer or part of an IC wafer. The substrate can be part of an integrated circuit such as a memory, a processing unit, an input/output device, etc.

[0028] In process 100 (FIGURE 1) at step 52, gate structures are formed by providing a gate stack including a gate dielectric layer 18 above a top surface 46 of layer 16, a gate conductor 22, and a bottom anti-reflective (BARC) layer 26. Top surface 46 can be considered a top surface of the substrate or wafer associated with portion 12, even though surface 46 corresponds to the top surface of layer 16 in FIGURE 2. In one embodiment, gate structures are formed directly above substrate 14 and layer 16 is not included.

[0029] Gate dielectric layer 18 can be a 5-30 Å thick layer of thermally grown silicon dioxide. Alternatively, layer 18 can be

deposited. Alternative materials for layer 18 include high-k dielectric layers, medium-k dielectric layers, silicon nitride, and other insulative materials.

[0030] Gate conductor 22 is preferably a polysilicon layer having a thickness of 1000-2000 Å and deposited by chemical vapor deposition (CVD). Gate conductor 22 can be deposited as a P-doped or N-doped layer. Alternatively, conductor 22 can be a metal layer such as a refractory metal layer deposited by CVD or sputtering.

[0031] Layer 26 is preferably an anti-reflective coating material such as silicon oxynitride (SiON) or silicon nitride (Si_3N_4). Alternative materials for layer 26 can also be utilized. Layer 26 serves a dual purpose of providing anti-reflective properties (e.g., as a BARC layer) as well as protecting gate conductor 22 during etching steps. Layer 26 is preferably deposited above gate conductor 22 by chemical vapor deposition (CVD) and has a thickness of between approximately 100 and 300 Å. Alternatively, layer 26 can be thermally grown.

[0032] Photoresist feature 24 is formed above layer 26. Preferably, photoresist feature 24 is lithographically patterned to form a gate structure from gate conductor 22 and dielectric layer 18.

[0033] In FIGURE 3, layers 26 and 18 and gate conductor 22 are etched in a conventional process to leave gate structure 38 (step 52 of process 100). Gate structure 38 can include spacers 23 formed in a deposition and etch back process. In one embodiment, spacers 23 are silicon dioxide, silicon nitride, or another insulating material. In a preferred embodiment, spacers 23 are silicon nitride and layer 26 is stripped before spacers 23 are formed. Substrate 14 and layer 16 can be doped to provide appropriate regions such as halo regions, channel regions, and source and drain regions in step 52.

[0034] In one embodiment, spacers 23 are not provided until after the sealing layer is provided. In another embodiment, layer 16 is doped to form shallow source and drain extensions (lightly doped) drains (LDD) before spacers 23 are provided and before the sealing layer is provided.

[0035] In FIGURE 4, in accordance with step 52 of process 100, bottom anti-reflective coating layer (BARC) 26 can be removed from gate conductor 22. BARC layer 26 is preferably removed for appropriate silicidation of gate conductor 22. In one embodiment, portions of spacers 23 are also removed so that a top surface of spacer 23 is planar with a top surface of gate conductor 22. BARC layer 26 can be removed using either a wet etching process with a phosphoric acid bath or by using a dry etching process.

[0036] In FIGURE 5, a layer 47 is provided above top surface 46 of layer 16 and gate structure 38. In an embodiment in which gate structure 38 is provided directly above substrate 14, layer 47 is provided above substrate 14 and gate structure 38. Layer 47 can be a buffer layer. Preferably, layer 47 is an insulative material suitable for semiconductor processing materials.

[0037] In one example, layer 47 is a 50-400 Å thick layer of silicon dioxide provided above gate structure 38 and silicon nitride spacers 23. Layer 47 can be a 100 Å thick silicon dioxide layer deposited in a tetraethylorthosilicate (TEOS) process. In another embodiment, layer 47 can be a masking material such as silicon nitride (Si_3N_4) or siliconoxynitride (SiON). Layer 47 provides an interface between layer 16 and gate structure 38 and the sealing layer discussed below. The sealing layer can prevent germanium outgassing and germanium resputtering following the implantation and annealing process.

[0038] In FIGURE 6, a layer 64 is provided above layer 47. Layer 64 serves as a sealing layer and is provided in accordance with step 56 of process 100. The combination of layers 47 and 64 form a sealing structure to prevent germanium outgassing and germanium resputtering. Layer 47 ensures good seating for layer 64.

[0039] In one embodiment, layer 64 is a layer of conductive or semiconductive material having a thickness of between approximately 50 and 200 Å. In one embodiment, layer 64 can be a layer of tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), titanium/ titanium nitride (Ti/TiN). Layer 64 can be deposited by sputtering or by CVD. The materials for layer 64 are chosen for their relatively high temperature stability and etch capabilities. Preferably, layers 47 and 64 are deposited in a low temperature process (e.g., less than approximately 800°C) to reduce germanium outgassing associated with layer 16 and substrate 14. For example, layer 64 may be deposited using a reactive sputtering or CVD process.

[0040] In another alternative embodiment, multiple layers similar to layer 64 can be provided to enhance the sealing effect. Layer 64 can have a thickness of between approximately 50 and 300 Å, and preferably approximately 200 Å.

[0041] In FIGURE 7, the substrate is doped in accordance with step 58 of process 100. Preferably, non-neutral dopants are implanted into layer 16 or substrate 14 to form source and drain regions 32. Source and drain regions 32 can include source and drain extensions 33 provided underneath spacers 23. Preferably, the non-neutral dopants include at least one of boron difluoride (BF_2), boron (B), arsenic (As), and phosphorous (P). Back sputter of germanium due to the implant

represented by arrow 66 is reduced via the sealing effect associated with layers 47 and 64.

[0042] In accordance with step 60 of process 100, layer 16 is annealed to activate dopants in source and drain regions 32. Preferably, a rapid thermal anneal (RTA) is performed at a temperature above approximately 600°C. According to a preferred embodiment, the RTA is performed at a temperature of approximately 1000°C for a period of between approximately 5 and 10 seconds. Layers 47 and 64 advantageously prevent germanium outgassing during annealing.

[0043] After high temperature processes associated with portion 12 are completed, layers 47 and 64 can be removed from portion 12 and conventional integrated circuit processes can be utilized to complete portion 12. In one embodiment, layers 47 and 64 are removed by dry etching processes. Alternatively, other removal processes can be utilized. In one preferred embodiment, a wet etch process is utilized to remove layer 64 followed by either a wet etch or a dry etch process to remove layer 47.

[0044] In one embodiment, portion 12 can be provided above a silicon-on-insulator (SOI) substrate. The stress in the buried oxide layer associated with the silicon-on-insulator substrate can be modified. The modified stress in the buried oxide layer of the silicon-on-insulator substrate modifies the stress associated with the top silicon layer. The stress in the buried oxide layer can be modified by implanting germanium through the top silicon layer into the buried oxide layer. The stress in the top silicon layer caused by the modified stress in the buried oxide layer improves carrier mobility in the top silicon layer, e.g., forms a strained silicon layer.

[0045] In another embodiment, portion 12 can be provided on a strained silicon-on-insulator substrate manufactured according to an advantageous process. The advantageous process uses plasma enhanced chemical vapor deposition (PECVD) to deposit a silicon dioxide film with compressive stress on a silicon substrate. A handling wafer or handle wafer is oxidized and bonded to the PECVD film and substrate. The substrate is then removed using a Smart Cut™ process, leaving a thin silicon layer on the PECVD oxide. The silicon layer on the PECVD oxide is in tensile stress, thereby operating as a strained layer.

[0046] It is understood that although the detailed drawings, specific examples, and particular values given provide exemplary embodiments of the present invention, the exemplary embodiments are for the purpose of illustration only. The method and apparatus in the aforementioned embodiments are not limited to the precise details and descriptions disclosed. For example, although particular sealing materials are described, other types of sealing materials can be utilized. Various changes may be made to the details disclosed without departing from the scope of the invention which is defined by the following claims.